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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/512,051 | 11/10/2004 | Akihiko Ito | 2593-0150PUS1 | 8417 |

2292 7590 08/22/2005

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| EXAMINER | |
|---|---|
| VELEZ, ROBERTO | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2829 | |

DATE MAILED: 08/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/512,051 | ITO ET AL. | |
| | Examiner | Art Unit | |
| | Roberto Velez | 2829 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/21/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1-3, 6-7 are rejected under 35 U.S.C. 102(e) as being anticipated by ***Saito (US Pat. 6,573,739).***

Regarding claim 1, ***Saito*** discloses an IC testing apparatus, for conducting a test by pressing input/output terminals of electronic devices [IC] to be tested against contact portions [51] of a test head [104] by a moving means [205, 302, 402] while said electronic devices [IC] to be tested are loaded on an electronic device conveying medium [304, 404], comprising: one or a plurality of said moving means [205, 302, 402] capable of gripping and conveying to and from said contact portions [51] a plurality of said electronic device conveying media loaded with said electronic devices [IC] to be tested at a time (Column 4, Lines 27-49 and Column 7, Lines 44-54).

Regarding claim 2, ***Saito*** discloses (Column 4, Lines 46-52) moving means [205, 302] capable of freely selecting the gripping number within the

number able to be gripped. It will pick up as many IC chips wanted to be tested during the process.

Regarding claim 3, ***Saito*** shows (Fig.1), one moving means [302, 402] capable of freely selecting the gripping number being independent from other moving means [205]. It can be seen in Fig. 1, that moving means [302, 402, 205] operate independently at the same time, because they perform different processes.

Regarding claim 6, ***Saito*** discloses (Column 4, Lines 27-30) moving grips said electronic device conveying medium loaded with said electronic devices to be tested and moves from a loading position [300] of pre-test electronic devices to said contact portions [51].

Regarding claim 7, ***Saito*** discloses (Column 7, Lines 49-54) moving grips said electronic device conveying medium loaded with said electronic devices to be tested and moves from said contact portions [51] to a loading position [400] of pre-test electronic devices to said contact portions [51].

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 6/4, 7/4 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Saito (US Pat. 6,573,739)*** in view of ***Yamashita et al. (US Pat. 6,339,321).***

Regarding claim 4, ***Saito*** discloses everything claimed above, in claim 1.

***Saito*** fails to disclose any two or more moving means among said plurality of moving means having a substantially overlapping operation range on a contact group as a set of said contact portions. However, ***Yamashita et al.*** shows (Fig. 3), moving means among said plurality of moving means [205b, 204b] having a substantially overlapping operation range on a contact group [203] as a set of said contact portions.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of ***Yamashita et al.*** into the device of ***Saito*** by using one single rail, as shown in ***Yamashita et al.*** (Fig. 3 [rail 205a]), instead of using two rails, as shown in ***Saito*** (Fig. 1 [301,401]). That way, all the arms can reach the contact group, overlapping the operation range. The ordinary artisan would have been motivated to modify ***Saito*** in the manner set forth above for at least saving time to resolve the process in a faster way, and at the same time using the whole operation range.

Regarding claim 6/4, ***Saito*** and ***Yamashita et al.*** disclose everything claimed, as applied above, in addition **Saito** discloses moving grips said electronic device conveying medium loaded with said electronic devices to be tested and moves from a loading position [300] of pre-test electronic devices to said contact portions [51] (Column 4, Lines 27-30).

Regarding claim 7/4, ***Saito*** and ***Yamashita et al.*** disclose everything claimed, as applied above, in addition **Saito** discloses moving grips said electronic device conveying medium loaded with said electronic devices to be tested and moves from said contact portions [51] to a loading position [400] of pre-test electronic devices to said contact portions [51] (Column 7, Lines 49-54).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over ***Saito (US Pat. 6,573,739)*** in view of ***Nemoto et al. (US Pat. 6,066,822).***

Regarding claim 5, ***Saito*** discloses everything claimed above, in claim 1.

***Saito*** fails to disclose said electronic device conveying medium is a strip format or a wafer. However, ***Nemoto et al.*** shows (Fig. 12), conveying medium [108] is a strip format.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of ***Nemoto et al.*** into the device of ***Saito*** by using an electronic device-conveying medium. The ordinary artisan would have been motivated to modify ***Saito*** in the manner set forth above to provide continuous supply of components for test, thereby increasing the speed of testing each component.

Claims 5/4, 8/4, 9/8/4, and 10/8/4 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Saito (US Pat. 6,573,739)*** and ***Yamashita et al. (US Pat. 6,339,321)*** and further in view of ***Nemoto et al. (US Pat. 6,066,822).***

Regarding claim 5/4, ***Saito*** and **Yamashita et al.** disclose everything claimed above, with the exception of *the* electronic device-conveying medium

being a strip format or a wafer. However, ***Nemoto et al.*** shows (Fig. 12), conveying medium [108] is a strip format.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of ***Nemoto et al.*** into the device of ***Saito*** and **Yamashita et al.** by using an electronic device-conveying medium. The ordinary artisan would have been motivated to modify ***Saito*** in the manner set forth above to provide continuous supply of components for test, thereby increasing the speed of testing each component.

Regarding claim 8/4, ***Saito*** and **Yamashita et al.** disclose everything claimed above, with the exception of a sum of the numbers of contact portions in said test head is $2^n$, where n is a natural number. However, ***Nemoto et al.*** discloses (Column 6, Lines 49-57), "the number of IC elements which may be connected with the tester head [104] at a time depends on the number of IC sockets mounted on the tester head [104]".

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of ***Nemoto et al.*** into the device of ***Saito*** by using a test head with the intentions of having as many contact portions as number of IC to be tested. The ordinary artisan would have been motivated to modify ***Saito*** in the manner set forth above for at least testing the IC elements all at one time.

Regarding claims 9/8/4 and 10/8/4, ***Saito*** and **Yamashita et al.** disclose everything claimed above, with the exception of a sum of the numbers of contact portions in said test head is $2^5$ and $2^6$. However, ***Nemoto et al.*** discloses

(Column 6, Lines 49-57), "the number of IC elements which may be connected with the tester head [104] at a time depends on the number of IC sockets mounted on the tester head [104]".

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of ***Nemoto et al.*** into the device of ***Saito*** by using a test head with the intentions of having as many contact portions as number of IC to be tested, in this case $2^5$ and $2^6$. The ordinary artisan would have been motivated to modify ***Saito*** in the manner set forth above for at least testing $2^5$ and $2^6$ IC elements all at one time.

Claim 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Saito (US Pat. 6,573,739)*** in view of ***Nemoto et al. (US Pat. 6,066,822).***

Regarding claim 8, ***Saito*** discloses everything claimed above, in claim 1.

***Saito*** fails to disclose a sum of the numbers of contact portions in said test head is $2^n$, where n is a natural number. However, ***Nemoto et al.*** discloses (Column 6, Lines 49-57), "the number of IC elements which may be connected with the tester head [104] at a time depends on the number of IC sockets mounted on the tester head [104]".

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of ***Nemoto et al.*** into the device of ***Saito*** by using a test head with the intentions of having as many contact portions as number of IC to be tested. The ordinary artisan would have been motivated to modify ***Saito*** in the manner set forth above for at least testing the IC elements all at one time.

Regarding claim 9-10, ***Saito*** discloses everything claimed above. ***Saito*** fails to disclose a sum of the numbers of contact portions in said test head is $2^5$ and $2^6$. However, ***Nemoto et al.*** discloses (Column 6, Lines 49-57), "the number of IC elements which may be connected with the tester head [104] at a time depends on the number of IC sockets mounted on the tester head [104]".

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of ***Nemoto et al.*** into the device of ***Saito*** by using a test head with the intentions of having as many contact portions as number of IC to be tested, in this case $2^5$ and $2^6$. The ordinary artisan would have been motivated to modify ***Saito*** in the manner set forth above for at least testing $2^5$ and $2^6$ IC elements all at one time.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

***Nakamura (US Pat. 6,248,967)*** discloses an IC testing apparatus. ***Nakamura*** discloses means for conducting a test by pressing input/output terminals of electronic devices [IC] to be tested against contact portions [26] of a test head [104] by a moving means [205, 302, 402] while said electronic devices [IC] to be tested are loaded on an electronic device conveying medium [304, 404], comprising: one or a plurality of said moving means [205, 302, 402] capable of gripping and conveying to and from said contact portions [26] a plurality of said electronic device conveying media loaded with said electronic devices [IC] to be tested at a time.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberto Velez whose telephone number is (571) 272-0218. The examiner can normally be reached on 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (571) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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